REMARKS

In response to the Office Action mailed October 12, 2007, Applicants respectfully request reconsideration. Claims 1-5 and 30-45 were previously pending in this application. Claims 1 and 2 have been amended herein. As a result, claims 1-5 and 30-45 remain pending for examination with claims 1, 2, 30 and 42 being independent. No new matter has been added.

Rejections Under 35 U.S.C. §103

A. Independent Claim 1

The Office Action rejected claim 1 under 35 U.S.C. 103(a) as being purportedly unpatentable over Richards (US 6,756,976) in view of Glennon (US 6,359,654), and further in view of Wu (US 6,414,689). Applicants respectfully request reconsideration.

The Office Action states that the limitation "same pixel position offset value" is interpreted to mean that the pixel position offset value is a constant (page 8). The Office Action further states that Wu describes that a row address for a screen line is offset from a "prior" row address by the same constant value. Based on the stated claim interpretation, Applicants assume that the Office Action is relying upon Wu to the extent that Wu's device displays an image in a position that corresponds with the position at which the image is stored in memory, and the relative positions of the displayed image and the memory storage location does not change. According to the line of reasoning as set forth in the Office Action, Wu's device refers to a location in memory using a single address and offset value. Since Wu's image display position corresponds with Wu's memory storage position, Wu's device displays a pixel based on the information stored in a corresponding memory position, because the relationship between the pixel position and the memory storage position does not change over time. If Applicants' understanding of the reasoning set forth in the Office Action is inaccurate, Applicants respectfully request clarification.

In response, claim 1 has been amended to remove the term "same pixel position offset value." Claim 1 as amended recites, inter alia, providing a cyclic succession of pixel position offset values comprising a first pixel position offset value, and for each row address providing a

new row address corresponding to said row address offset by the first pixel position offset value and activating pixels of a screen line associated with said new row address, based on the read states of the row associated with said row address. Wu does not teach or suggest activating pixels of a screen line associated with a new row address based on the read states of the row associated with said row address. Wu does not provide a new row address because Wu's image is displayed at a position that corresponds with the position in which the image is stored in memory.

In addition or in the alternative, claim 1 also recites providing new states corresponding to the read states of the memory points of the frame memory row associated with said new row address, said read states being offset by the first pixel position offset value and activating pixels of a screen line associated with said row address based on the new states. Wu does not teach or suggest activating pixels of a screen line associated with a row address based on new states, where the read states are offset by a pixel position offset value. Rather, as discussed above, Wu's image is displayed at a position that corresponds with the position in which the image is stored in memory. Richards and Glennon fail to remedy these deficiencies of Wu. In view of the foregoing, claim 1 patentably distinguishes over any combination of Richards, Glennon and Wu. Accordingly, withdrawal of this rejection is respectfully requested.

B. Independent Claim 2

The Office Action rejected claims 2, 4, and 5 under 35 U.S.C. 103(a) as being purportedly unpatentable over Richards, in view of Glennon, further in view of Leung (US 5,900,887), and further in view of Wu. Applicants respectfully request reconsideration.

Applicants have amended claim 2 to remove the term "same pixel position offset value." Claim 2 as amended recites, *inter alia*, a cyclic succession of pixel position offset values comprising a first pixel position offset value; and a dedicated address circuit receiving the address of the row read by the read means and transmitting to the row driver a new address corresponding to the address of the read row offset by the first pixel position offset value, and/or a dedicated state circuit receiving the states of the points read by the read means and transmitting to the column driver new states corresponding to the read states offset by the first pixel position offset value. Wu does not teach or suggest transmitting to the row driver a new address corresponding to the address of the read row offset by a first pixel position offset value.

Furthermore, Wu does not teach or suggest transmitting to a column driver new states corresponding to read states offset by the first pixel position offset value. Rather, as discussed above, Wu's image is displayed at a position that corresponds with the position in which the image is stored in memory. Richards, Glennon and Leung fail to remedy these deficiencies of Wu. Therefore, claim 2 patentably distinguishes over any combination of these references. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 3-5 depend from claim 2 and are therefore patentable for at least the same reasons.

Rejections Under 35 U.S.C. §102

A. Independent Claim 30

The Office Action rejected claims 30, 35 and 37 under U.S.C. 102(e) as purportedly being anticipated by Miyachi, U.S. Patent No. 6,937,224. Applicants respectfully traverse these rejections.

Miyachi describes an LCD display technique (Col. 1, lines 10-23). FIG. 31 of Miyachi illustrates an active matrix LCD device in which a single horizontal line of an image signal is sampled into a sampling memory 2 and stored into holding memory 3 (Col 1, lines 11-16). The horizontal line is then displayed by being first converted into an analog signal by D/A converter 4, and then the analog signal is used to drive the pixels of the selected horizontal line (Col. 1, lines 16-24). Miyachi states that the above operation is performed for all of the horizontal lines of the image in sequence so that the entire image can be displayed (Col. 1, lines 25-28, Col. 6, lines 1-7).

The Office Action relies upon holding memory 3 of Miyachi as purportedly being the "second memory" of Applicants' claim 30. The Office Action states that the holding memory 3 of Miyachi "shifts storage locations at which the row of image data is stored in second storage locations of the second memory (3), the second storage locations being shifted with respect to the first storage locations." (Page 4). Applicants respectfully disagree because Miyachi makes no mention of shifting storage locations within a memory, such as holding memory 3. The Office Action cites Col. 5, lines 50-58, Col. 5, lines 1-7 and Col. 1, lines 12-20 as purportedly describing the shifting of storage locations within holding memory

3. However, the cited passages of Miyachi at Cols. 5 and 6 make no mention of a memory, but rather describe the activation of row and column line drivers to display an image. The cited passage of Miyachi at Col. 1 states that a horizontal line of image data is stored into the sampling memory 2 and the holding memory 3, however, this passage makes no mention that either of these memories shift the storage locations at which image data is stored in the memories.

By contrast, claim 30 recites, *inter alia*, that the second memory shifts storage locations at which the row of image data is stored based on the column offset value such that the row of image data is stored in second storage locations of the second memory, the second storage locations being shifted with respect to the first storage locations. Miyachi does not teach or suggest a memory that shifts storage locations at which a row of image data is stored. In view of the foregoing, claim 30 patentably distinguishes over Miyachi. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 31-41 depend from claim 30 and are therefore patentable for at least the same reasons.

B. Independent Claim 42

The Office Action rejected claims 42-45 under 35 U.S.C. 102(e) as being purportedly anticipated by Choi (US0020030076332A 1). Applicants respectfully traverse these rejections.

The Office Action relies upon controller 104 of Choi as purportedly being the control circuit recited in claim 42, and relies upon operation unit 105 of Choi as purportedly being the "logic unit." The Office Action states, "Since the display is shifted after the same image is displayed, this means that the logic unit [sic] previously received a first row address corresponding to a row of image data .... So, logic unit receives first row address corresponding to a row of image data and performs operation on first row address using row offset value to determine second row address that is offset from first row address." Applicants respectfully disagree. First, Choi contains no mention of an address, much less performing an operation on a first address to determine a second address. Second, the Office Action appears to assume that operation unit 105 uses addresses to access memory 102 and performs an operation on the addresses to move the image. Applicants respectfully disagree because FIG. 1 of Choi shows that operation unit 105 of Choi is not connected to the memory 102. Rather, as illustrated in FIG. 1 of Choi, the image is

written to and read from memory 102 by signal processor 101. Choi states that the operation unit 105 operates the display unit to display the image in the desired position, based on the control signal from controller 104 (¶¶ 40-41). Choi further states, "The operation unit 105 operates the display unit 106 in the same way an existing display device does." (¶ 41). Therefore, operation unit 105 moves the image by operating the display unit, not by performing calculations on addresses to obtain new addresses.

By contrast, claim 42 recites, *inter alia*, a control circuit that provides a row offset value to the logic unit; wherein the logic unit receives a first row address corresponding to a row of the image data and performs an operation on the first row address using the row offset value to determine a second row address that is offset from the first row address. Choi does not teach or suggest a control circuit that provides a row offset value to a logic unit. Choi also does not teach or suggest a logic unit that performs an operation on a first row address to determine a second row address. In view of the foregoing, claim 42 patentably distinguishes over Choi. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 43-45 depend from claim 42 and are therefore patentable for at least the same reasons.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

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